

Using dsPIC30F A/D Converters and the DSP library for Signal Filtering

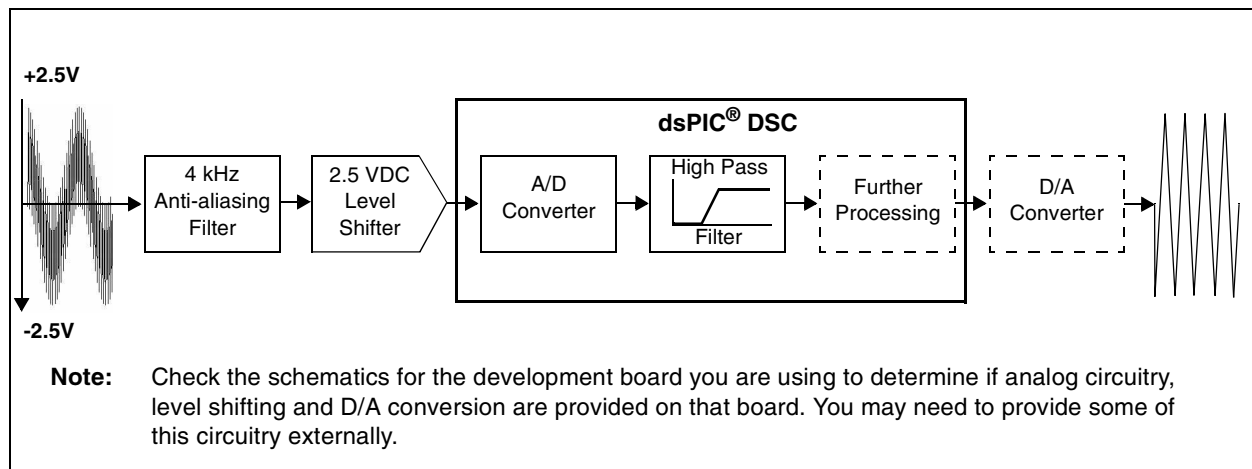
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OVERVIEW

This Code Example document briefly describes and demonstrates the capabilities of the dsPIC30F Digital Signal Controller product family for performing signal analysis and filtering. The accompanying MPLAB® IDE workspace exemplifies why applications that require

signal analysis and filtering will benefit from the dsPIC30F product family. Key features in the dsPIC30F architecture that enable such applications are briefly described to help you understand the example source code. We will summarize how the example source code demonstrates these capabilities. We will also provide a list of the software and hardware development tools and libraries used in building the example project.

FIGURE 1: SIGNAL ANALYSIS AND FILTERING WITH dsPIC® DSC



BENEFITS

The dsPIC® DSC devices feature a DSP engine that is seamlessly integrated into the CPU. They also provide an on-chip 10-bit (1M SPS) or 12-bit (200K SPS) A/D Converter peripheral module. This combination of the A/D converter peripheral module and DSP engine allows applications to perform complex operations like signal filtering and frequency estimation with the dsPIC DSC. This capability reduces on-board analog circuitry, saves space on the board and provides the additional benefits of field re-programmability and improving temperature characteristics of your circuit.

OPERATION

The example dsPIC30F project in the attached MPLAB IDE workspace demonstrates how the dsPIC30F A/D converter can be configured for converting an analog signal and providing a signed fractional (1.15 format)

digital result to an Infinite Impulse Response (IIR) filter. IIR filters can be used to attenuate or amplify a range of frequencies from an incoming signal.

The Digital IIR filter used in this example is a C-callable function provided in the dsPIC30F DSP library software. Such digital filters are typically implemented in software using Multiply-Accumulate (MAC) class of DSP instructions, featured in the dsPIC DSC architecture. The MAC-class of instructions requires input data to be presented in 1.15 signed-fractional number format. The 1.15 format is described in detail in the *dsPIC30F Programmer's Reference Manual* (DS70030). The dsPIC30F A/D converters provide conversion results in many number formats, including the 1.15 signed fractional format. Further details on the dsPIC30F A/D converters may be found in the *dsPIC30F Family Reference Manual* (DS70046).

Figure 1 illustrates the operation of the dsPIC30F device demonstrated by the example project.

The example dsPIC30F project configures the dsPIC30F A/D converter for a sampling analog input pin, AN7, at a rate of 8 kHz. Any single-ended input signal band-limited to 4 kHz may be applied on the input pin. A single-ended input signal (not differential) is one that has a DC bias that is half the reference voltage.

The A/D converter is set up for interrupting the CPU after converting 16 samples. At each interrupt, a High-Pass Elliptic IIR filter function is invoked. The high-pass filter heavily attenuates any signals in the frequency range, 0 to 500 Hz. The filtering is performed on a block of 16 samples using a cascade of transposed biquadratic (Direct Form II) IIR filter sections provided by the DSP library. The biquadratic filter section is a commonly used filter topology that implements the difference equations required for filtering a digital signal.

DEVELOPMENT TOOLS AND LIBRARIES

The example workspace was created using MPLAB IDE v7.11. All source code in the project is written in C. Source-level comments have been provided to aid understanding. The project also uses an IIR filtering function from the DSP Library archive file, `libdsp-coff.a`, which is provided in the MPLAB C30 v1.32 C compiler tools suite. The IIR filter uses filter coefficients generated by dsPIC DSC Filter Design, a graphical tool that designs digital filters for the dsPIC30F device. The example MPLAB IDE workspace is configured for a dsPIC30F6014 device, but it is easily re-configured for any dsPIC30F device with a 10-bit or 12-bit A/D converter. Analog input pin, AN7, used in this project is available for use on all dsPIC DSC development boards and many dsPIC DSC devices.

The project/workspace assumes that a 7.37 MHz crystal provides device clocking. Such crystals are provided on several dsPIC30F development boards, for example dsPICDEM™ 64-Pin Starter Development Board, dsPICDEM 1.1, dsPICDEM 2, dsPICDEM.net™, and dsPICDEM MC1. Additional oscillator and PLL options have been configured in source code to operate the device at a throughput of 29.4 MIPS. All Microchip software tools and dsPIC30F documentation described in this document can be downloaded from <http://www.microchip.com>.

SUMMARY

The example project lets you set up the dsPIC30F 12-bit A/D converter for sampling an analog input signal at 8 KHz in an interrupt-driven fashion using C language. The example also demonstrates how you can invoke an IIR filter function provided in the dsPIC30F DSP library software, as well as, how coefficients generated by the dsPIC DSC Filter Design software can be incorporated into the project. dsPICworks™ tool and dsPIC DSC Filter Design screen shots and simulation files are also provided in the Zip file. Refer to the `Readme.txt` file for a summary description of the various files and folders provided in the project. Operational aspects are described in source-level comments in each file.

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